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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,381	08/17/2001	Serge Lasserre	TI-31354	4434

23494 7590 03/25/2003

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EXAMINER
BRAGDON, REGINALD GLENWOOD

ART UNIT	PAPER NUMBER
2188	6

DATE MAILED: 03/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,381	LASSERRE, SERGE	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 17 August 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The Information Disclosure Statement(s) received 17 August 2001 has been considered. Please see the attached PTO-1449(s).

Drawings

3. The drawings are objected to because:

In figure 6, "505(0)" should be --506(0)--.

In figure 10, there is no element "1504". See page 26, paragraph 68.

In figure 13B, there is no element "2028". See page 30, paragraph 84.

4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The abstract of the disclosure is objected to because it is longer than 150 words. Correction is required. See MPEP § 608.01(b).

6. Applicant is requested to update any data (continuation serial number, patent number, etc...) concerning co-pending or related applications listed in the specification.

The status/serial numbers of the application on page 1 should be updated.

The status/serial number of the application on page 11 should be updated.

7. The disclosure is objected to because of the following informalities:

On page 15, paragraph 28, "signals 524" should be --signals 514--.

In table 2 on page 22, the superscript "1" is utilized in several locations, but is not further identified.

On page 28, last line "in" should be --In--.

Appropriate correction is required.

Claim Objections

8. Claim 12 is objected to because of the following informalities: in line 8, "location" should be --segment--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3, 5-9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hassoun et al. (5,557,622).

As per claim 1, with reference to figures 1-2, Hassoun et al. teaches a processor 30 and a cache 80 ("local memory") which is connected to the processor over the local bus 60. The cache includes a plurality of blocks ("plurality of segments"). See column 2, lines 30-32. A cache control unit includes a plurality of locations in a storage device which maintains a tag and status bits ("indicator bit") for each block. See column 2, lines 32-40. See also figure 3 for a description of the tag and status bits stored in the cache controller. The cache controller 440 (see figures 2 and 4) includes circuitry to perform direct memory accesses (DMA) on a cache fill operation ("operable to transfer data to a selectable portion of segments...from a selectable region of a second memory"). See column 7, lines 6-9. Hassoun et al. also teaches updating the status bits in the tag storage on the cache fill operation. See column 7, lines 9-12.

As per claim 2, Hassoun et al. teaches that the status bits include valid bits, and that on a cache fill operation the cache controller updates the status bits of a new block to valid. See column 7, lines 9-12.

As per claim 3, Hassoun et al. teaches that if the block is not valid, then a cache miss is indicated. This indicates that hit/miss circuitry ("miss detection circuitry") is located within the cache controller. See column 6, lines 53-55 and figure 2. Hassoun et al. further teaches that while waiting for access from the main memory for the data that missed, then the memory request from the processor remains pending on the local bus (i.e. the processor stalls until valid data is returned). See column 6, lines 55-61.

As per claim 5, Hassoun et al. teaches that if the block is not valid, then a cache miss is indicated. This indicates that hit/miss circuitry ("miss detection circuitry") is located within the cache controller. See column 6, lines 53-55 and figure 2. Hassoun et al. further teaches a cache fill operation where an address is output to the memory to access data using a DMA operation and data is returned to the cache memory using the DMA operation. See column 7, lines 6-12.

As per claim 6, Hassoun et al. teaches that if the data is valid in the cache, then it would not be necessary to perform a DMA access to retrieve the data from the main memory. See column 2, lines 52-54.

As per claim 7, Hassoun et al. teaches storing dirty bits in the tag storage. See figure 3 and column 4, line 16.

As per claim 8, Hassoun et al. teaches that if a dirty bit is set in the tag storage for a particular block, then a DMA operation is performed to transfer the data back to memory. See column 7, lines 20-24. If the block is not dirty, then the valid bit associated with the block is reset, thus invalidating the block and not transferring the block back to memory. See column 7, lines 18-20.

As per claim 9, Hassoun et al. teaches that if the processor writes to a block in the cache memory, then the dirty bit is set for that block. See figure 4 and column 10, lines 9-11, where it is taught that one of the transactions performed on the status bits is "make valid and dirty".

As per claim 12, with reference to figures 1-2, Hassoun et al. teaches a processor 30 and a cache 80 ("local memory") which is connected to the processor over the local bus 60. The cache includes a plurality of blocks ("plurality of segments"). See column 2, lines 30-32. A cache control unit includes a plurality of locations in a storage device which maintains a tag and status

bits ("associating a plurality of indicator bits") for each block. See column 2, lines 32-40. See also figure 3 for a description of the tag and status bits stored in the cache controller. The cache controller 440 (see figures 2 and 4) includes circuitry to perform direct memory accesses (DMA) on a cache fill operation. See column 7, lines 6-9. Hassoun et al. also teaches updating (i.e. "setting") the status bits in the tag storage on the cache fill operation. See column 7, lines 9-12. Hassoun et al. teaches that the status bits include valid bits, and that on a cache fill operation the cache controller updates the status bits of a new block to valid. See column 7, lines 9-12.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hassoun et al.

As per claim 4, Hassoun et al. does not teach timeout circuitry operable to interrupt the processor if the DMA circuitry does not validate the first segment within a certain period of time. It would have been obvious to one of ordinary skill in the art to have incorporated timeout circuitry to interrupt the processor if the DMA circuitry does not return the requested data within a certain period of time because this would maintain efficient operation of the system for high priority processor operations.

As per claim 10, Hassoun et al. does not teach a mode circuit which in one mode transfers only dirty segments and in another mode transfers the entire block. However it would have been obvious to one of ordinary skill in the art to have modified Hassoun et al. to incorporate a mode circuit such that in one mode transfers only dirty segments and in another mode transfers the entire block because this would increase the flexibility of the system. Hassoun et al. already teaches transferring to memory only dirty blocks. Incorporating the ability to transfer plural blocks without referring to the main memory would permit fast cache flushing on context changes.

As per claim 11, Hassoun et al. does not teach that the system is embodied in a cellular telephone. However it would have been obvious to one of ordinary skill in the art to have incorporated the system of Hassoun et al. into a cellular phone because this would create a versatile cellular phone system.

Conclusion

13. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)

or

(703) 746-7239 (Official Communications)

(703) 746-7240 (For Status inquiries, draft communications)

and/or

(703) 746-5693 (Use this FAX#, only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal page/amendment be faxed directly to them on occasion).

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
March 20, 2003